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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,933	08/13/2004	Jui-Hsiang Pan	11537-US-PA	4932

31561 7590 12/16/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER
MANDALA, VICTOR A

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 12/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/710,933	PAN ET AL.	
	Examiner	Art Unit	
	Victor A. Mandala Jr.	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 16-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 16-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I in the reply filed on 11/29/05 is acknowledged.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the chips that are wire bonded to the chip carrier must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, 6, & 7 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,534,879 Terui.

3. Referring to claim 1, a quad flat no-lead package structure, comprising: a chip carrier, (Figure 3B #10), having a top surface and a bottom surface, wherein a plurality of conductive leads, (Figure 3B #30 & 40), is disposed on the bottom surface of the chip carrier, (Figure 3B #10), while a plurality of pads, (Figure 3B #81, 83, 85, & 87), is disposed on the top surface of the chip carrier, (Figure 3B #10), the conductive leads, (Figure 3B #30 & 40), being electrically connected to the pads, (Figure 3B #81, 83, 85, & 87); and at least a chip, (Figure 3B #60), disposed on the top surface of the chip carrier, (Figure 3B #10), and electrically connected, (Figure 3B #90), to the chip carrier, (Figure 3B #10).

4. Referring to claim 2, a package structure as claimed in claim 1, further comprising a passivation layer, (Col. 5 Lines 20-22), to cover the chip, (Figure 3B #60).

5. Referring to claim 3, a package structure as claimed in claim 1, wherein the chip carrier, (Figure 3B #10), includes an interconnect layer, (Figure 3B #95), between the pads, (Figure 3B #81, 83, 85, & 87), and the conductive leads, (Figure 3B #30 & 40), and

wherein the interconnect layer, (Figure 3B #95), includes at least a via, (Figure 3B #95), for connecting one of the pads, (Figure 3B #81, 83, 85, & 87), and one of the conductive leads, (Figure 3B #30 & 40).

6. Referring to claim 4, a package structure as claimed in claim 1, wherein the chip, (Figure 3B #60), is electrically connected to the chip carrier, (Figure 3B #10), through wire bonding technology, (Figure 3B #90).

7. Referring to claim 6, a package structure as claimed in claim 1, wherein the chip, (Figure 3B #60), is electrically connected to the chip carrier, (Figure 3B #10), through surface mount technology, (Col. 12 Lines 64-67).

8. Referring to claim 7, a package structure as claimed in claim 6, wherein an anisotropic conductive paste, (Col. 12 Lines 64-67), is further included to attach the chip, (Figure 3B #60), and the chip carrier, (Figure 3B #10).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 5, 16-18 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,261,467 Giri et al.

9. Referring to claim 1, a quad flat no-lead package structure, comprising: a chip carrier, (Figure 1 #114), having a top surface and a bottom surface, wherein a plurality of conductive leads, (Figure 1 #122), is disposed on the bottom surface of the chip carrier, (Figure 1 #114), while a plurality of pads, (Figure 1A #118), is disposed on the top

surface of the chip carrier, (Figure 1 #114), the conductive leads, (Figure 1 #122), being electrically connected to the pads, (Figure 1A #118); and at least a chip, (Figure 1 Chip), disposed on the top surface of the chip carrier, (Figure 1 #114), and electrically connected, (Figure 1A #C4), to the chip carrier, (Figure 1 #114).

10. Referring to claim 3, a package structure as claimed in claim 1, wherein the chip carrier, (Figure 1 #114), includes an interconnect layer, (Figure 1 #126), between the pads, (Figure 1A #118), and the conductive leads, (Figure 1 #122), and wherein the interconnect layer, (Figure 1 #126), includes at least a via, (Figure 1 #124), for connecting one of the pads, (Figure 1A #118), and one of the conductive leads, (Figure 1 #122).

11. Referring to claim 5, a package structure as claimed in claim 1, wherein the chip, (Figure 1 Chip), is electrically connected to the chip carrier, (Figure 1 #114), through flip chip technology.

12. Referring to claim 16, a wafer-level package structure, comprising: a wafer, (Figure 1 #114), having a plurality of sections, (Col. 1 Lines 50-52); a plurality of conductive blocks, (Figure 1 #122 or 121), disposed on the wafer, (Figure 1 #114), and in each of the sections of the wafer, (Figure 1 #114); a metal interconnect layer, (Figure 1 #126), connecting the plurality of the conductive blocks, (Figure 1 #121 or 122), wherein the metal interconnect layer, (Figure 1 #126), comprises at least a via hole, (Figure 1 #124), and a plurality of pads, (Figure 1A #118), wherein the via hole, (Figure 1 #124), electrically connects one of the conductive blocks, (Figure 1 #121 or 122), and one of the pads, (Figure 1A #118), and wherein the pads, (Figure 1A #118), are disposed on an uppermost surface of the metal interconnect layer, (Figure 1 #126); and at least a chip,

(Figure 1 Chip), disposed onto each of the sections of the wafer, (Figure 1 #126), wherein the chip, (Figure 1 Chip), includes a plurality of bonding pads, (Figure 1A #118), that are correspondingly connected to the pads, (Figure 1A #118).

13. Referring to claim 17, a wafer-level package structure of claim 16, further comprising a passivation layer, (Figure 1 #112), covering each section of the wafer, (Figure 1 #126).

14. Referring to claim 18, a wafer-level package structure of claim 16, wherein the metal interconnect layer, (Figure 1 #126), further includes an oxide layer, (Figure 1 #108 and Col. 4 Lines 26 & 49-53), between the conductive blocks, (Figure 1 #121 or 122), and the pads, (Figure 1A #118), while the via hole, (Figure 1 #124), through the oxide layer, (Figure 1 #108), connects one of the conductive blocks, (Figure 1 #121 or 122), and one of the pads, (Figure 1A #118).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A. Mandala Jr. whose telephone number is (571) 272-1918. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VAMJ
12/7/05

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800